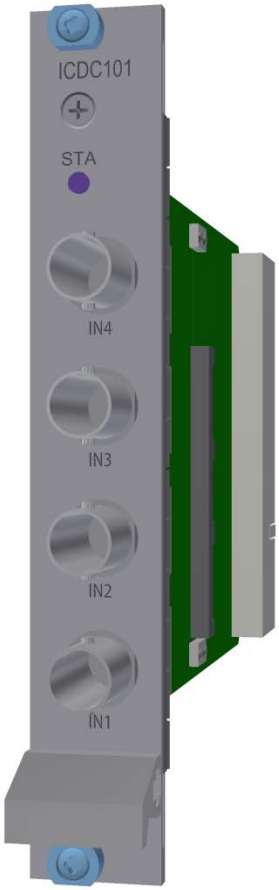
Features

- 4 channel analog interface TEDS4BNC
  4 widely accepted BNC front connectors
  *u*ltra *w*ide *D*ynamic inputs cover every signal
    1V to 23V input-voltage range ($8.5V_{eff}$)
    Low noise (typically $3\mu V_{20Hz\text{-}20kHz}$ input-referred)
    15kΩ input resistance
  4x 4.7mA center contact current supply
  Capable of reading and writing TEDS inside sensors
    IEEE1451.4 Class 1 MMI, shared signal wire
- Simultaneous 30bit A/D-conversion at 48/96/192kS/s
  Auto-calibration for offset reduction
- Advanced Record-Trigger capability
  Adjustable between start and end of recording
  Activated by software, hardware or input-voltage
- 32bit recording makes gain-setting obsolete
- 1.5GB cPCI-independent onboard real time memory
  16MS / input for up to 349s recording time (48kS/s)
- Concurrent cPCI-streaming up to the limits of the harddisk (96/192kS/s down-sampled to 48kS/s)
- Nonvolatile calibration and configuration memory
- Onboard voltage and temperature monitoring
- Full Color RGB status LED (marked STA)
- Low power consumption (6W typically)



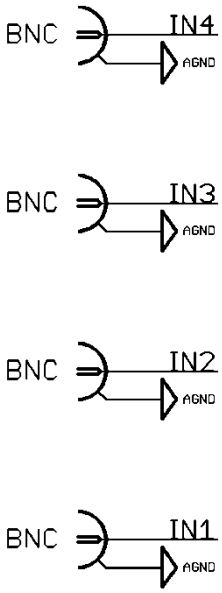
BNC front connector scheme

Description

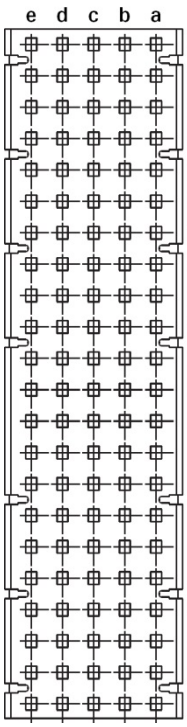
The ICDC101 is a low noise 3U 4HP cPCI slot-in card with automatic offset-calibration, offering 4 *u*ltra *w*ide *D*ynamic 1V to 23V inputs for the common 2…20mA current supplied sensors better known by their registered trademarks ICP®, DeltaTron®, Isotron® and Piezotron®.

Plugged sensors are recognized and in case they have a transducer electronic data sheet (TEDS) inside it can be read and written. Each of the 4 ICDC101 channels utilizes a combination of two advanced multi-bit delta-sigma analog-to-digital-converter channels to achieve an overall A/D-resolution of 30bit for outstanding 131dB(A)

dynamic. Concurrent capabilities allow for high-channel recording with many cards (1.5GB onboard RAM) and longtime streaming. Results of the factory-gain-calibration are stored in a nonvolatile memory and used for compensation while measuring.

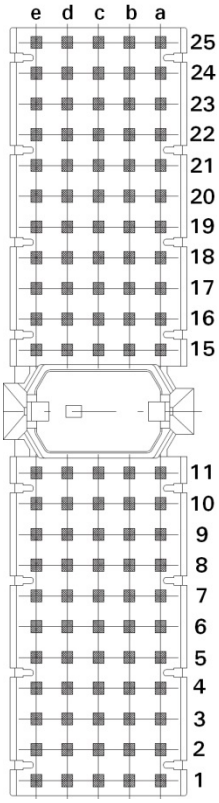


cPCI J2 connector scheme (not standardized)



e	d	c	b	a
AGND	RC_ENA	AGND	PGA0	PGA1
AGND	GND	AGND	PGA2	PGA3
AGND	PGA4	AGND		
+6V5	GND	AGND		
+6V5	RS2_TX	+6V5	GND	/RS2_TX
+6V5	GND	+6V5	/RS2_RX	
+6V5	RS2_RX	+6V5	GND	
	GND		/ENA_RECTRIG	
	RS1_RX_TTL	VIO	GND	
RS2_TX_TTL	GND		/ENABLE	
	RS1_TX_TTL	VIO	GND	
RS2_RX_TTL	GND		/SHUTTER	
	/RECTRIGGER	VIO	GND	
	GND	AUXIOP3	/STOPSTREAM	
		VIO	GND	
	GND	AUXIOP2	/SYNCHRONIZE	FPGA_TDO
FPGA_TCK		VIO	GND	FPGA_TDI
FPGA_TMS	GND	AUXIOP1		VIO
/FPGA_CE	FPGA_CONF_DONE	+3V3	GND	
/FPGA_CS	/FPGA_CONFIG	FPGA_DCLK	24576KHZ	
FPGA_ASD	FPGA_DATA	+3V3	GND	

cPCI J1 connector scheme (standardized)

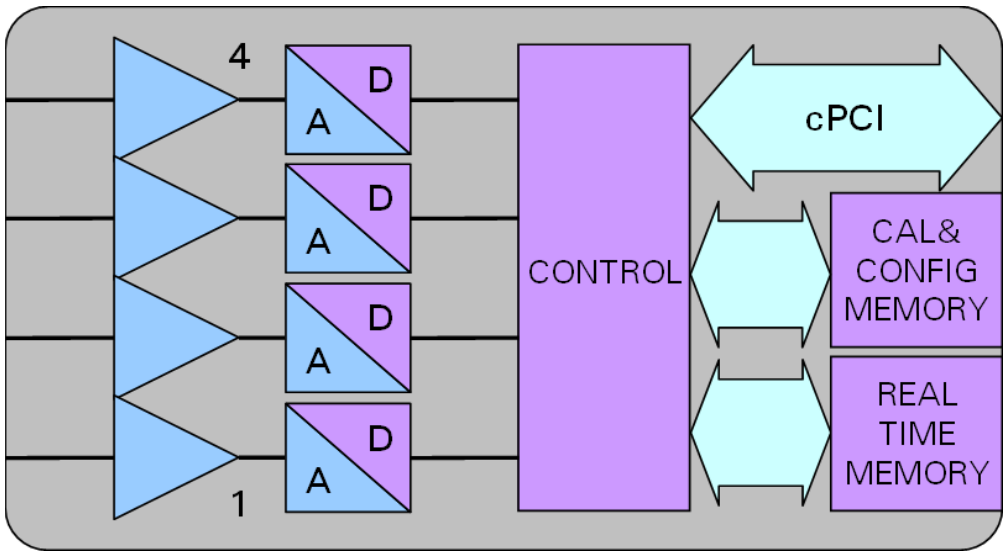


e	d	c	b	a
+5V	+3V3			+5V
	AD0	VIO	+5V	AD1
AD2	+5V	AD3	AD4	+3V3
AD5	AD6	+3V3	GND	AD7
C/BE0	M66EN	AD8	AD9	+3V3
AD10	AD11	VIO	GND	AD12
AD13	GND	AD14	AD15	+3V3
C/BE1	PAR	+3V3	GND	/SERR
/PERR	GND			+3V3
/LOCK	/STOP	VIO	GND	/DEVSEL
/TRDY		/IRDY	/FRAME	+3V3

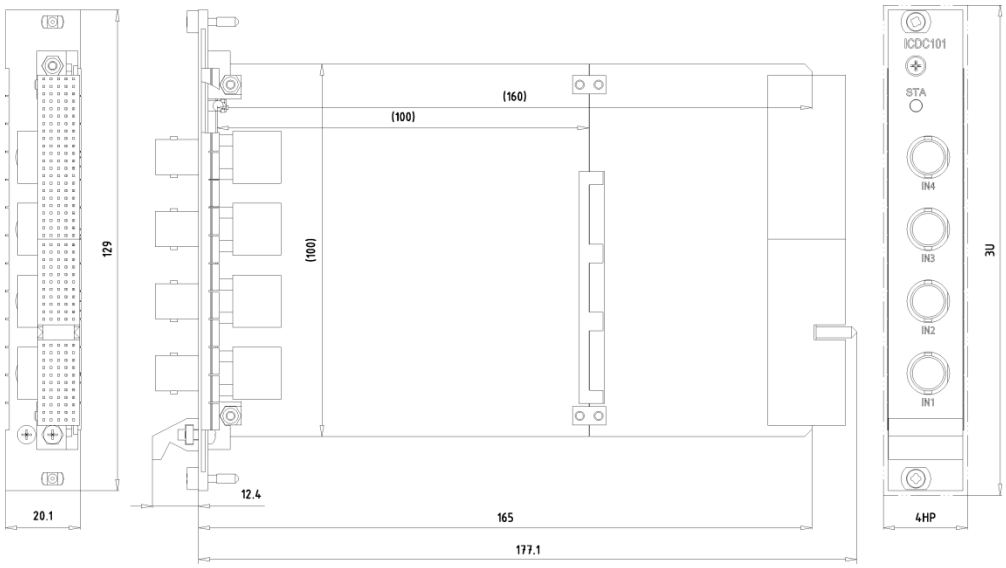
blanks are not connected on the card

C/BE2	GND	AD16	AD17	AD18
AD19	AD20	+3V3	GND	AD21
AD22	GND	AD23	IDSEL	C/BE3
AD24	AD25	VIO	GND	AD26
AD27	GND	AD28	AD29	AD30
AD31	CLK	+3V3	GND	/REQ
/GNT	GND	/RST		
		VIO		
	+5V			/INTA
TDI	TDO		+5V	
+5V	+12V		-12V	+5V

Block diagram



Mechanical data



Weight 206g

Absolute maximum ratings

Parameter		Min	Max	Unit	Remarks
Power	+6V5 to AGND	-0.3	8	V	Stresses above these may cause permanent damage. This is a stress rating only; functional operation at these or any other conditions above is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Only one absolute maximum rating may be applied at any one time.
	+5V to GND	-0.3	6	V	
	+3V3 to GND	-0.3	4	V	
	VIO to GND	-0.3	4	V	
Analog inputs to AGND*		-12	24	V	
Digital inputs to GND		-0.3	4	V	
Storage temperature		-50	125	°C	

* Since the inputs are especially designed to fit to current supplied sensors like ICP®, special care must be taken to ensure ±100mA current limitation in measuring mode (0V to 24V) and TEDS mode (-12V to 0V).

Conformity

Electrical safety	complies with DIN EN 61010-1
Electromagnetic compatibility (EMC)	complies with DIN EN 61326

Operating conditions

Parameter		Min	Typ	Max	Unit	Remarks
Power supply	(+6V5)	6.3	6.5	6.7	V	voltages at the cPCI connectors J1+J2 must be guaranteed to be within these limits
	(+5V)	4.7	5.0	5.3	V	
	(+3V3)	3.0	3.3	3.6	V	
	(VIO)	3.0	3.3	3.6	V	
Sensor supply (front)4.7mA		3.7	4.7	5.7	mA	at center contact of each BNC connector, short-circuit-proof
Analog inputs	IN to AGND	1		23	V	with current supplied sensor in measuring mode
	IN to AGND	-5		0	V	with current supplied sensor in TEDS mode
/SHUTTER and	low	0		1	V	both these and also /STOPSTREAM must be pulled-up with 220Ω resistors to VIO on the backplane
/RECTRIGGER	high	2		3.3	V	
Temperature		0		70	°C	the air surrounding the card must be within these limits
Relative humidity		10		80	%	not to be operated until condensation is evaporated

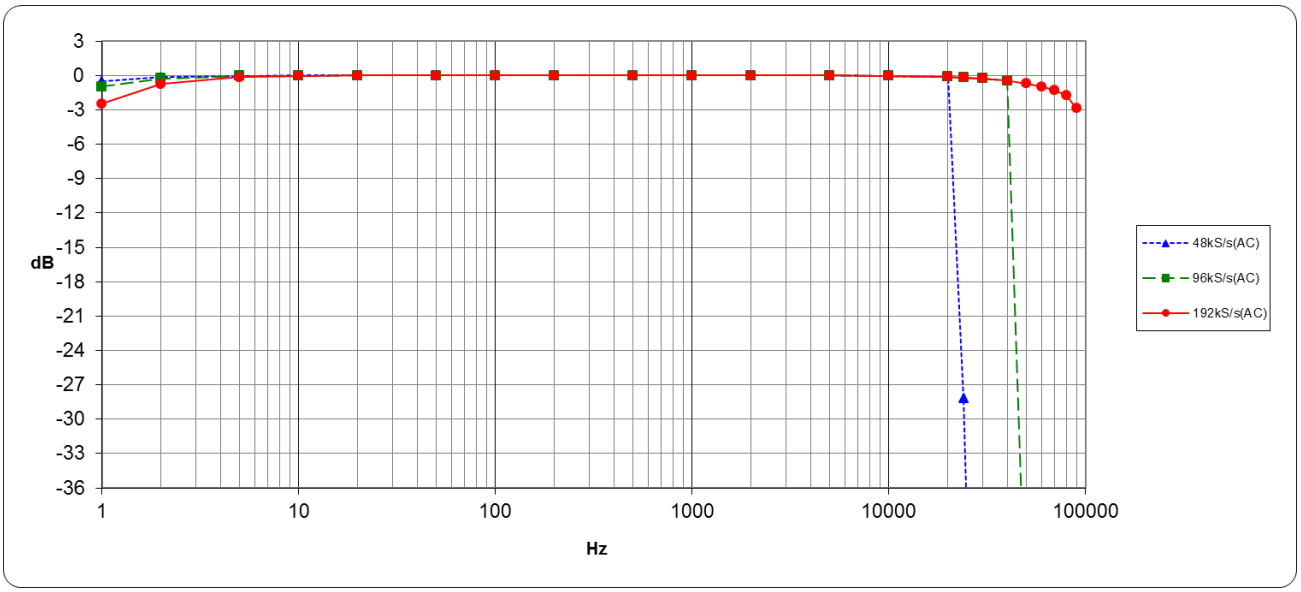
All other inputs and outputs are of the LVTTL-type (max-low=0.7V, min-high=1.7V).
/ENA_RECTRIG, /ENABLE and /SYNCHRONIZE must be pulled-up with 1kΩ resistors to VIO on the backplane.
24576kHz is an input and shall be connected to a stable and accurate clock-source.
AGND and GND are not connected on the card.
AGND and GND shall be connected only once in the mainframe.

Electrical characteristics

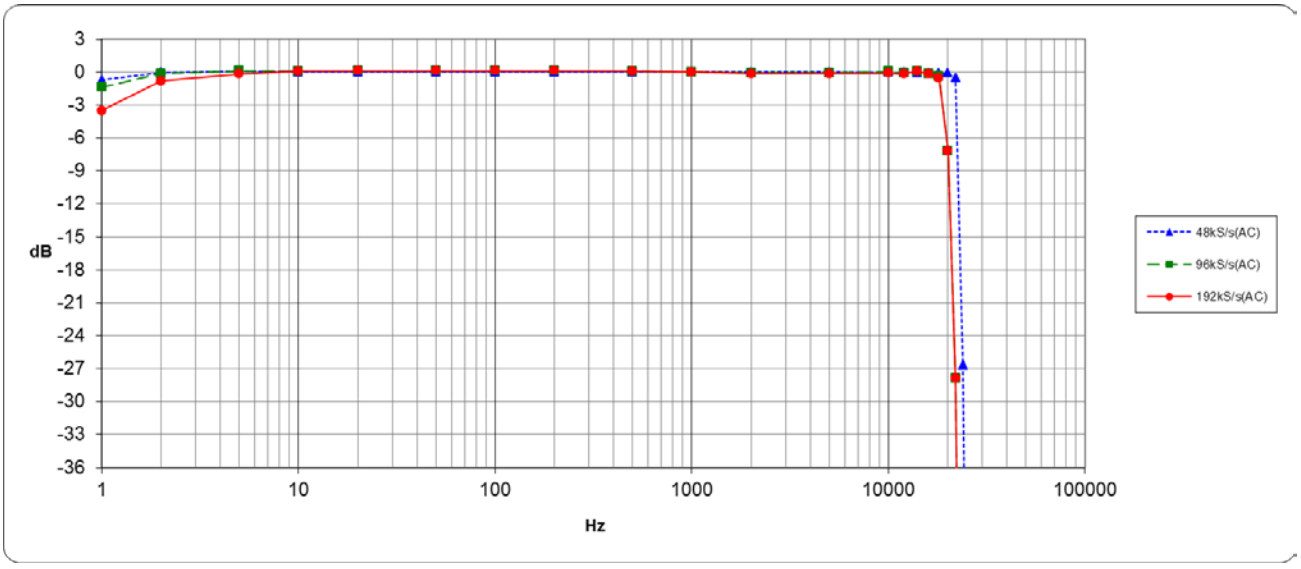
Parameter	Min	Typ	Max	Unit	Condition
Full-scale input-voltage	7.8	8.5	9.2	V_{eff}	
Input-resistance	14795	15771	15928	Ω	
Input referred noise		3.5	5.6	μV_{eff}	
@ 48kS/s		3.3	5.6	μV_{eff}	
@ 96kS/s		3.3	5.6	μV_{eff}	inputs connected to 50Ω resistors, 20Hz…20kHz-weighted
@ 192kS/s					
Dynamic range @ 48kS/s (A-weighted)	127	131		dB(A)	
@ 48kS/s (20Hz…20kHz-weighted)	124	128		dB	
@ 96kS/s (A-weighted)	127	131		dB(A)	
@ 96kS/s (20Hz…20kHz-weighted)	124	128		dB	
@ 96kS/s (20Hz…40kHz-weighted)	120	125		dB	full-scale input related to noise with inputs connected to 50Ω resistors
@ 192kS/s (A-weighted)	127	131		dB(A)	
@ 192kS/s (20Hz…20kHz-weighted)	124	128		dB	
@ 192kS/s (20Hz…40kHz-weighted)	120	125		dB	
@ 192kS/s (20Hz…80kHz-weighted)	118	122		dB	
Total harmonic distortion + noise		-68	-66	dB	
@ 48kHz		-68	-66	dB	most distorted channel
@ 96kHz		-67	-66	dB	@ input 1kHz, $5V_{eff}$,
@ 192kHz					20Hz…20kHz-weighted
Accuracy Offset-error		656	8192	LSB	worst channel @ 192kS/s,
Input referred offset-error		3.69	46	µV	inputs connected to 50Ω resistors
Channel separation					most disturbed channel related to
Crosstalk @ 1kHz (800Hz…1250Hz-weighted)		-101	-100	dB	driven channel @ input $5V_{eff}$,
Crosstalk @ 10kHz (8000Hz…12500Hz-weighted)		-99	-80	dB	192kS/s,
					other channels connected to 50Ω
Power supply current (+6V5)		693	1000	mA	measured with 100mΩ shunt-
(+5V)		255	500	mA	resistors
(+3V3)		248	300	mA	@ 192kS/s,
(VIO)		3	20	mA	inputs connected to 50Ω resistors
Power consumption (+6V5)		4.30	6.60	W	
(+5V)		1.28	2.65	W	supply currents from above,
(+3V3)		0.79	1.04	W	voltages measured between
(VIO)		0.01	0.07	W	shunt-resistors and card
(total)		6.38	10.36	W	

Frequency response

Record-mode



Streaming-mode



uwD and how the user benefits from it

When it comes to measuring noise, vibration and other physical values spanning more than the human ear can capture noise in the upper frequency range is of concern for the measurement system. Unfortunately very few high-resolution A/D-converters reveal their noise behavior in the range above 20kHz, therefore our engineers had to gain experience over the years investigating in a lot of measurements. So far they think they have found the best single-chip 192kHz 24bit A/D-converter on the market, put it in the series of ADC10x Measurement Cards and were happy when they measured up to 121dB(A) dynamic and still 107dB at 20Hz to 80kHz because it was more than needed to cover the whole dynamic of the capsules we use in our microphone-arrays. Then our customers asked for additional inputs to connect their current supplied sensors like ICP® with TEDS inside and we started to design a card for those. Right at the start we had to learn that 121dB(A) dynamic was not enough for some of the more expensive sensors of this kind. The classic approach would have been to make use of an amplifier with switchable gain but we spent too much time in repeating overdriven measurements and because we were certain that also for our customers – time is money – we caused our engineers some sleepless nights asking for something better. What they came out with we call *uwD*, which stands for *u*ltra *w*ide *D*ynamic. This innovation surpasses the limitations of the best on market single-chip 24bit A/D-converters by achieving 131dB(A) dynamic and still 122dB at 20Hz to 80kHz.

Theory of operation

Signals entering the card at the BNC connectors are passing ESD-protections and line-inductors where high-frequency-components are removed that the following amplifiers cannot damp sufficiently. Relays are switching the inputs between amplifiers and TEDS interface (IEEE1451.4 Class 1 MMI, shared signal wire) and they also permit calibration by connecting the amplifiers to 50Ω resistors. Low noise current regulators on a 24V source provide for sensor supply and detection circuits are implemented to spot their presence. Each channel's amplifier utilizes a low noise CMOS circuit with two different amplifications precisely adjusted by 0.1% resistors. Capacitors set the lower end of the frequency range to <1Hz and the upper end to >100kHz. A total attenuation of 48dB is achieved at half the oversampling-speed of the simultaneously sampling advanced multi-bit delta-sigma analog-to-digital-converters – low aliasing-distortions are the benefit. The converters offer selectable reduction-low-pass-filters for 48, 96 and 192kHz output rate. The digital control unit collects the serial 48bit data-streams from each converter's two channels and calculates a level and frequency dependant combination thereof factoring in the ratio of the two different amplifications resulting in a virtual *u*ltra *w*ide *D*ynamic 30bit A/D-resolution followed by a filter where DC-offset is removed and output is optimized to 32bit words. Up to 16MS for each of the 4 inputs are stored in real time memory; when full, oldest data is overwritten by the latest. Streaming via the cPCI bus is performed simultaneously; 48kS/s is sent directly, 96kS/s and 192kS/s are down-sampled to 48kS/s. End-point of recording can be between Record-Trigger and 349 seconds later. The Record-Trigger can be released by cPCI-command, pulling down /RECTRIGGER at J2 or reaching at least one of four cPCI-register definable values (one for each of the four input-channels). /SHUTTER is a pull-down-activated bidirectional control-signal; it is available at J2 and can be sensed and released through cPCI. /SHUTTER is recorded in Bit0 of every channel and counted in a cPCI-register. Temperature-sensor, voltage-check, front-panel-RGB-LED and nonvolatile calibration and configuration memory are available to cPCI. During factory-calibration gains of all channels are measured and stored in this memory.

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